original patent claims 1-11, which are also part of this reissue application. Applicants, therefore, respectfully request the Examiner also examine original patent claims 1-11 and provide his disposition thereof.

Applicants have amended the specification to correct typographical and grammatical errors. Applicants have amended claims 19, 30-33, 36, and 46 to more appropriately define their invention.

Applicants have also added new claims 47-72 to further define the subject matter of their invention. As a result, claims 1-72 are pending. In accordance with 37 C.F.R. § 1.121(b)(2)(iii), Applicants provide the following explanation of the support in the patent disclosure for the amended new claims. Each of amended claims 19, 30-33, 36, and 46 and new claims 47-72 are supported in the patent disclosure at column 3, lines 46-column 4, line 54 which describes the circuit shown in Fig. 3 and its operation. Additionally, claim 49 is further supported at column 6, lines 51-56, and claim 71 is further supported at column 5, lines 5-16.

In the Office Action, the Examiner objected to the reissue declaration for failing to comply with 37 C.F.R. § 1.175(a)(1) and (a)(2), and lacking the statement "all error." The Examiner also rejected claims 12-46 because the reissue declaration was objected to.

For a reissue declaration, section 1.175(a)(1) requires a statement that "[t]he applicant believes the original patent to be wholly or partly inoperative or invalid by reason of the patentee claiming more or less than the patentee had the right to claim in the patent, stating at least one error being relied upon as the basis for reissue." Consistent with that requirement, Applicants declared in the reissue declaration that "we verily believe that through error, without any deceptive intent, the said patent is partly inoperative or invalid by reason of our claiming less

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than we had a right to claim." Applicants identified the error as "claiming less than we had a right to claim" and proceeded to provide a specific example of such error. Applicants explained that they "did not appreciate that the claimed 'plural capacitive elements' could be claimed more broadly without running afoul of the prior art." The reissue declaration clearly complied with 37 C.F.R. § 1.175(a)(1).

Section 1.175(a)(2) additionally requires the reissue declaration state that "[a]ll errors being corrected in the reissue application up to the time of filing of the oath or declaration under this paragraph arose without any deceptive intention on the part of the applicant."

Applicants stated in the reissue declaration that "[t]he errors relied on arose during prosecution, and were found during a post-issuance study of the technology and the '526 patent. **The errors arose without deceptive intent.**" (emphasis added) These statements represent that all errors of which Applicants have become aware arose without deceptive intent. Applicants therefore respectfully submit that the requirement of 37 C.F.R. 1.175(a)(2) has been met.

Therefore, Applicants respectfully request the withdrawal of the objection to the reissue declaration and the rejection of claims 12-46 based on the Examiner's objection to the reissue declaration.

The Examiner also rejected claims 12-46 as being anticipated by *Masuda et al.* Claims 12-46 are not anticipated because *Masuda et al.* fails to disclose all elements of any claim.

With reference to the embodiment illustrated in Figs. 1 and 2, *Masuda et al.* discloses a load capacitor $C_0$ is charged from and discharged to a power capacitor $C_1$ via an inductor L. Several SCR elements $S_0$, $S_1$, and $S_2$ are switched in the process. Inductor L is provided and sized so that upon closure of $S_0$, transient oscillation is generated in the circuit to charge $C_0$ to a

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voltage twice that of $C_1$. (col. 7, lines 26-33). Further, upon opening $S_0$ and closing $S_1$, $C_o$ is discharged to $C_1$ by transient oscillation. (col. 7, lines 33-37). Specific conditions for the transient oscillation, including criteria for an appropriate value for L are described at col. 8, line 12-51. $S_2$ is subsequently closed so that the remaining charge on $C_0$ is discharged. (col. 10, lines 19-42).

*Masuda et al.* states that it is necessary to choose L "to reduce the rising time and falling time" of the voltage applied to $C_0$. (col. 7, lines 50-54). Thus, the circuit is adapted to rapidly charge $C_0$.

This disclosed structure of *Masuda et al.* does not disclose all elements of Applicants' claim 12. For example, with reference again to Fig. 1 of *Masuda et al.* which is representative of the various embodiments disclosed therein, if it is assumed, *arguendo*, that $S_0$ and $S_1$ (or $S_2$) provided for charging and discharging the capacitive load correspond to Applicants' claimed first and second switches, and $C_1$ corresponds to Applicants' claimed charge storage element, there is **no** feature of *Masuda et al.* that corresponds to the claimed switch assembly to connect the charge storage element to the capacitive load. Viewed another way, both of $S_1$ and $S_2$ are provided for discharging $C_0$ and may arguably correspond to Applicants' claimed second switch. Then, $S_o$ is the **only** remaining switching element of *Masuda et al.* to meet elements of claim 12, while claim 12 still requires **both** the first switch **and** the switch assembly.

Therefore *Masuda et al.* does not disclose each and every element of claim 12 and for at least this reason claim 12 is not anticipated.

Additionally, claim 12 requires that the switch assembly connect the charge storage element to "gradually charge" the capacitive load. *Masuda et al.* does not disclose this claim

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requirement and instead expressly provides for rapid charging. See *Masuda et al.* at col. 7, line 50-54 and col. 9, lines 1-7. For this reason also, claim 12 is not anticipated by *Masuda et al.*

Since Applicants' independent claims 26 and 30 include limitations corresponding to those of claim 12 discussed above, independent claims 12, 26, and 30 and dependent claims 13-25 are not anticipated by *Masuda et al.*

*Masuda et al.* fails to disclose all elements of Applicants' independent claim 27. Claim 27 recites a method for charging and discharging a capacitive load from a voltage source. The method comprises steps of charging the capacitive load from the voltage source and discharging the capacitive load by connecting it through a switch assembly to at least one charge storage element. Thus, claim 27 at least covers an initial charging operation in accordance with the invention as described for an illustrated embodiment in Applicants' specification at col. 4, lines 18-34. In the illustrated embodiment, during initial charging, when first switch 14 (switch N in Fig. 3) is closed, charge is for the first time applied to the load capacitor 12. Subsequently, when switch N is opened and switch N-1 is closed, charge is transferred to the capacitor $C_T$ associated with switch N-1. These operations correspond to the steps of claim 27.

In contrast, *Masuda et al.* charges load capacitor $C_o$ from power capacitor $C_1$ by means of the transient oscillation with inductor L. Therefore, *Masuda et al.* at least fails to disclose a step of "charging said capacitive load with said voltage source" as required by claim 27. Therefore, claim 27 and claim 28 that depends therefrom are not anticipated by *Masuda et al.*

Applicants' independent claim 29 is not anticipated by *Masuda et al.* because it also recites a method including the same step as in claim 27 of charging said capacitive load with said voltage source." That step is not disclosed by *Masuda et al.*

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*Masuda et al.* fails to disclose all elements of independent claims 31 and 46 . These claims recite a system and method, respectively, for charging and discharging a capacitive load in N steps utilizing N-1 charge storage devices. *Masuda et al.* fails to disclose such features. Therefore, independent claims 31 and 46 and dependent claims 32-37 are not anticipated by *Masuda et al.*

*Masuda et al.* fails to disclose all elements of independent claim 38 because it fails to disclose a plurality of charge storage devices and a switching device operable to selectively couple the plurality of charge storage devices to the capacitive load. Instead, *Masuda et al.* only discloses the power capacitor $C_1$ that is connectable to load capacitor Co through inductor L. Therefore claim 38 and claims 39-44 that depend therefrom are not anticipated by *Masuda et al.*

*Masuda et al.* fails to disclose all elements of independent claim 45 because it at least fails to disclose the claimed step of "selectively coupling a charge storage device to the capacitive load to cause at least one of the charging and discharging . . . to occur in a plurality of steps." In contrast, *Masuda et al.* discloses rapid charging, effected by transient oscillations, that occurs in a single step. Therefore, independent claim 45 is not anticipated by *Masuda et al.*

Also in the Office Action, the Examiner rejected claims 12-46 under 35 U.S.C. § 103(a) as unpatentable over admitted prior art Fig. 2 of the above-identified application, in view of *Masuda et al.*, stating it would have been obvious to one of ordinary skill in the art at the time of the invention to "replace the voltage source of applicant's [sic] admitted prior art with the charge storage element of *Masuda et al.* in order to provide steady and cost effective power source."

When a prior art reference is modified for an "obviousness" rejection, there must have been a suggestion or motivation in the prior art to modify the prior art reference. MPEP 2143.01.

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The Examiner cites to no reference as motivation for the modification. The respective circuits disclosed in prior art Fig. 2 and *Masuda et* al. differ substantially. In particular, Masuda *et al.* describes an RLC circuit that generates transient oscillations to charge and discharge a load capacitor. The power capacitor $C_1$ only charges the load in conjunction with the inductor L so that charging can be rapidly achieved by transient oscillation. In contrast, prior art Fig. 2 discloses multiple separate voltage sources separately connectable to a capacitive load. The voltages of the multiple voltage sources are "evenly distributed" to enable charging of the load capacitor in multiple steps to reduce energy dissipation, based on the total energy dissipation of equation (3). See *Svensson et al.* at col. 3, lines 29-38. The circuits of *Masuda et al.* and prior art Fig. 2 fundamentally differ in kind and mode of operation and there is, therefore, no basis in either reference for motivating the modification proposed by the Examiner. Therefore, a person of ordinary skill would not modify the circuit of prior art Fig. 2 as proposed by the Examiner.

New claims 47-72 are patentable over *Masuda et al.* Each claim recites features not disclosed in *Masuda et al.*, including features disclosed above for various ones of rejected claims 12-46.

In view of the foregoing amendments and remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

To the extent if any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any fees due under

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37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

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